The 6th Reactive Synthesis Competition
SYNTCOMP 2019

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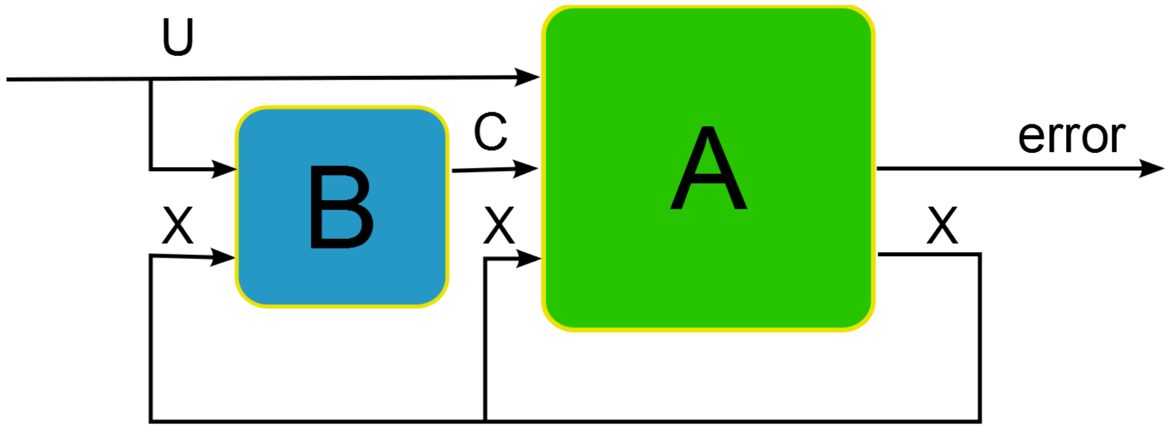
SCOS
Systematic Construction of Correct Systems

14 July 2019 - SYNT Workshop @ CAV

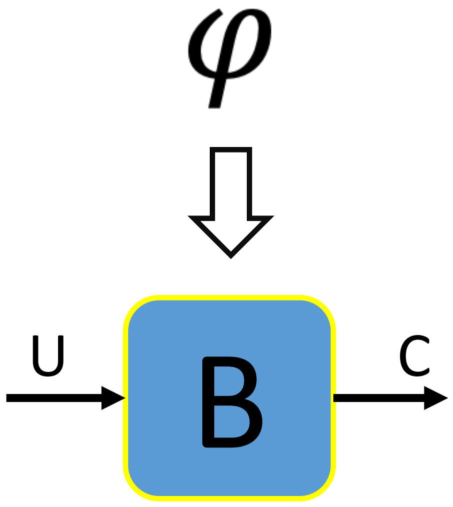
What is Reactive Synthesis?

We consider two variants: either

- synthesize circuit B for given circuit A in picture below (such that error is not raised for arbitrary sequence of Us), or
- synthesize circuit B that satisfies LTL formula φ on its inputs and outputs.

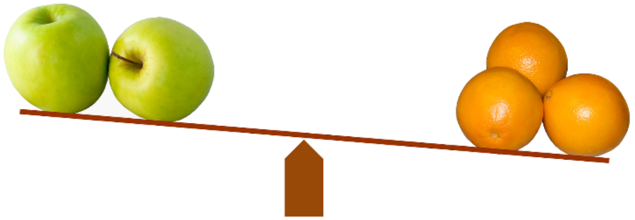


Safety (AIGER)



LTL (TLSF)

SYNTCOMP: Goals



Make reactive synthesis tools comparable:

- establish **benchmark format**
- collect **benchmark library**
- provide platform for **fair and comprehensive evaluation**

Guide development of reactive synthesis tools:

- encourage implementation of mature, **push-button tools**
- improve state of the art through **challenging benchmarks**

SYNTCOMP: History and Rules

First Competition: 2014 (Vienna Summer of Logic)

safety properties in AIGER-based format

Second Competition: 2015 (SYNT/CAV, San Francisco)

Third Competition: 2016 (SYNT/CAV, Toronto)

extension to LTL specs in TLSF

Fourth Competition: 2017 (SYNT/CAV, Heidelberg)

Fifth Competition: 2018 (SYNT/CAV @ FLoC, Oxford)

This year (SYNT/CAV, NY): **migrated to StarExec!**

Solver Input:

Specification in AIGER or TLSF

Solver Output:

Yes/No answer or implementation (in AIGER) that satisfies spec

Implementations are model checked

Ranking based on quantity and quality

Tools compete in up to 3 configurations per track

SYNTCOMP 2019: STAREXEC SET-UP

StarExec for Reactive Synthesis

- StarExec is a cross community logic solving service developed at the University of Iowa
- StarExec allows
  - community organizers to store, manage, make available benchmarks;
  - competition organizers to run logic solver competitions; and
  - community members to perform comparative evaluations of logic solvers on public or private benchmark problems.
- Sister competition SyGuS on StarExec since 2014

SYNTCOMP 2019: REALIZABILITY TRACKS

Participants 2019

Safety: Last year's easiest-to-migrate tools

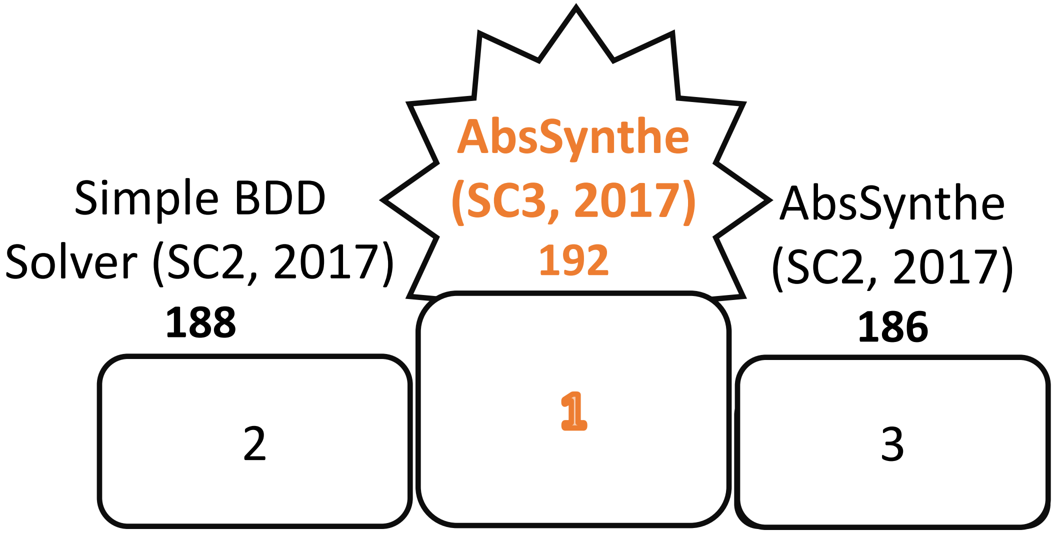
- **Simple BDD Solver** (Walker, Ryzhyk)
  - With change of options: SC2 = early exit when abstracting
- **AbsSynthe** (Brenguier, Perez, Raskin, Sankur) [SYNT14,15]

LTL: Updated tools

- **ltlsynt** (Duret-Lutz, Colange, Michaud)
  - Optimized LAR-based automaton construction fast but buggy ☹
- **Strix** (Meyer, Sickert, Luttenberger) [CAV18]
  - Implemented all LICS18 translations for LTL fragments
  - Implemented symbolic representation of the transition
  - Added an exploration strategy for the game arena (priority queue + heuristics)

Results: Realizability (Number of Solved Instances)

Safety - Sequential (1 CPU $\boldsymbol{hr}$, single core**)**



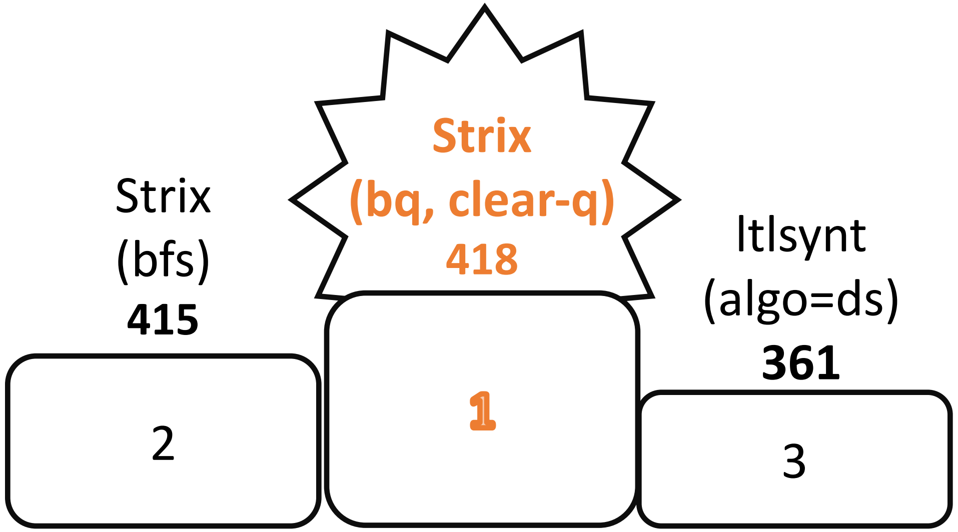
Simple BDD Solver (SC2, 2017)
188
2

AbsSynthe (SC3, 2017)
192
1

AbsSynthe (SC2, 2017)
186
3

Total Instances: 274

LTL - Sequential (1 CPU $\boldsymbol{hr}$, single core**)**



Strix (bfs)
415
2

Strix (bq, clear-q)
418
1

ltlsynt (algo=ds)
361
3

Total Instances: 434

New Benchmarks 2019

Safety (AIGER):

- Random examples (M. Sakr)
  - Uniformly sampled from all $\left(2^{2^{u+c+l}}\right)^{l} \cdot \left(2^{2^{l}}\right)$ specs, with u = no. of uncontrollable inputs, c = controllable, l = latches

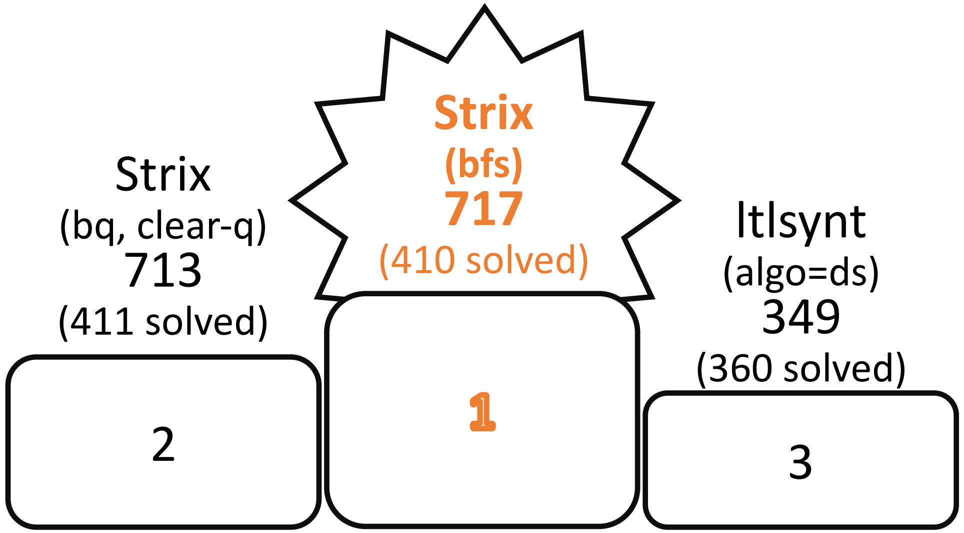
LTL (TLSF):

- Temporal Stream Logic (TSL) benchmarks (F. Klein, M. Santolucito)
  - Essentially discretization of TSL specs (e.g. kitchen timer spec)
- Parametric TLSF files with higher parameter values (S. Jacobs)
- Arcade-game-on-FPGA benchmarks (P. Heim, G. Geier)
  - Translated TSL spec to TLSF

SYNTCOMP 2019: SYNTHESIS TRACK

LTL (TLSF) Results: Synthesis (Quality Ranking)

Sequential mode (1 CPU hr, single core)



Strix

(bq, clear-q)

713

(411 solved)

Strix

(bfs)

717

(410 solved)

ltlsynt

(algo=ds)

349

(360 solved)

Total Instances: 434

LTL (TLSF) Results: Synthesis

Tool	Configuration	Quality Points	Solved Instances
ltlsynt	seqsynt1	337.315847	358
ltlsynt	seqsynt2	348.788475	360
ltlsynt	seqsynt3	361.297606	DISQUALIFIED (375)
Strix	parallel_synthesis_conf1	714.562706	411
Strix	parallel_synthesis_conf2	705.686036	411
Strix	sequential_synthesis_conf2	713.030335	411
Strix	sequential_synthesis_conf1	716.899591	410

Summary and Outlook

We are achieving our goals:

- Significant improvement in (LTL) tools
- Thousands of benchmarks collected
- Migration culled tools with active dev

Attracting new teams (generations):

- SYNTCOMP workshop/tutorial ETAPS'19
- Other venues?

Possible extensions/changes for next years:

- SYNTCOMP'20: parity-game track (PGSolver format)
- require counter-strategy if unrealizable?
- can we make life easier for LTL model checkers?

Winners of Safety Track:

	Sequential
Realizability	**AbsSynthe**

Winners of LTL Track:

	Sequential
Realizability	**Strix**
Synthesis Quality	**Strix**
Synthesis Quantity	**Strix**

More details soon on http://www.syntcomp.org and in the competition report!