



The 5th Reactive Synthesis Competition - SYNTCOMP 2018

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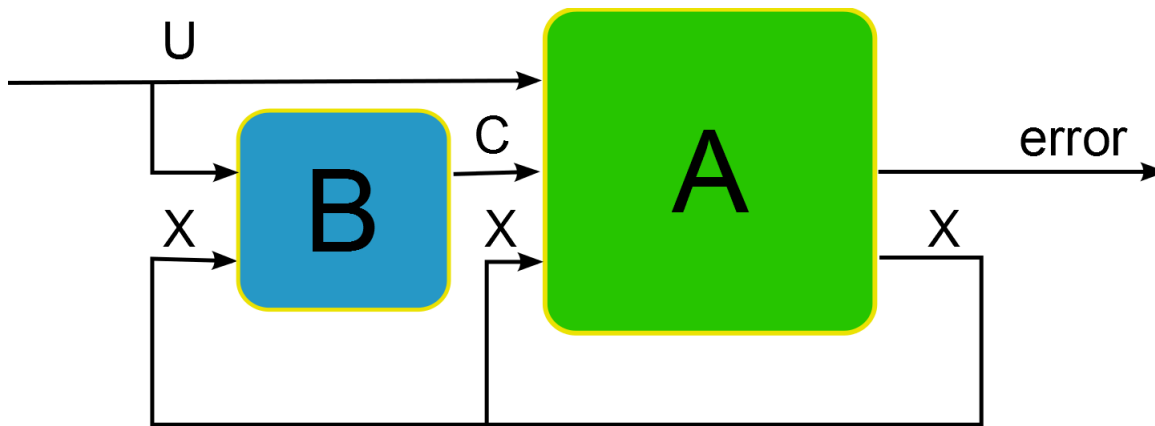


18 July 2018 – SYNT Workshop at FLoC, Oxford

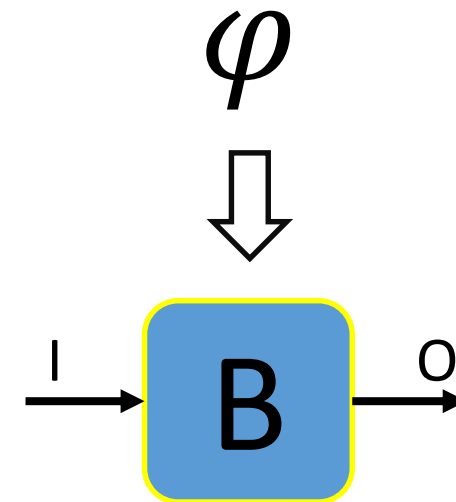
What is Reactive Synthesis?

We consider two variants: either

- synthesize circuit B for given circuit A in picture below (such that error is not raised for arbitrary sequence of Us), or
- synthesize circuit B that satisfies LTL formula φ on its inputs and outputs.



Safety (AIGER)

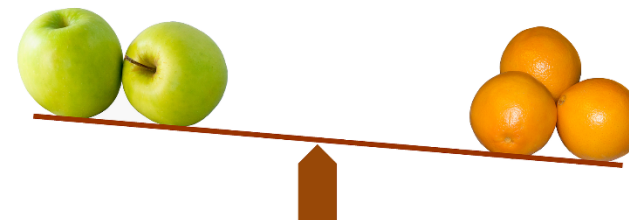


LTL (TLFS)

SYNTCOMP: Goals

Make reactive synthesis tools comparable:

- establish **benchmark format**
- collect **benchmark library**
- provide platform for **fair and comprehensive evaluation**



Guide development of reactive synthesis tools:

- encourage implementation of mature, **push-button tools**
- improve state of the art through **challenging benchmarks**

SYNTCOMP: History and Rules

First Competition: 2014 (Vienna Summer of Logic)

safety properties in ALGER-based format

Second Competition: 2015 (SYNT/CAV, San Francisco)

Third Competition: 2016 (SYNT/CAV, Toronto)

extension to LTL specs in TLSF

Fourth Competition: 2017 (SYNT/CAV, Heidelberg)

This year: Fifth Competition, same rules as last year

Solver Input:

Specification in ALGER or TLSF

Solver Output:

Yes/No answer or
Implementation (in ALGER) that
satisfies spec

Implementations

are model checked

**Ranking based on
quantity and quality**

**Tools compete in up to
3 configurations per track**

SYNTCOMP 2018: SAFETY (AIGER) TRACK

Safety (Aiger): Participants 2018

Updated:

- **Simple BDD Solver** (Walker, Ryzhyk): new portfolio configurations

Last Years best tools running again:

- **AbsSynthe** (Brenguier, Perez, Raskin, Sankur) [SYNT14,15]
- **Demiurge** (Könighofer, Seidl) [VMCAI14]
- **SafetySynth** (Tentrup)
- **TermiteSAT** (Legg, Narodytska, Ryzhyk) [CAV2016]

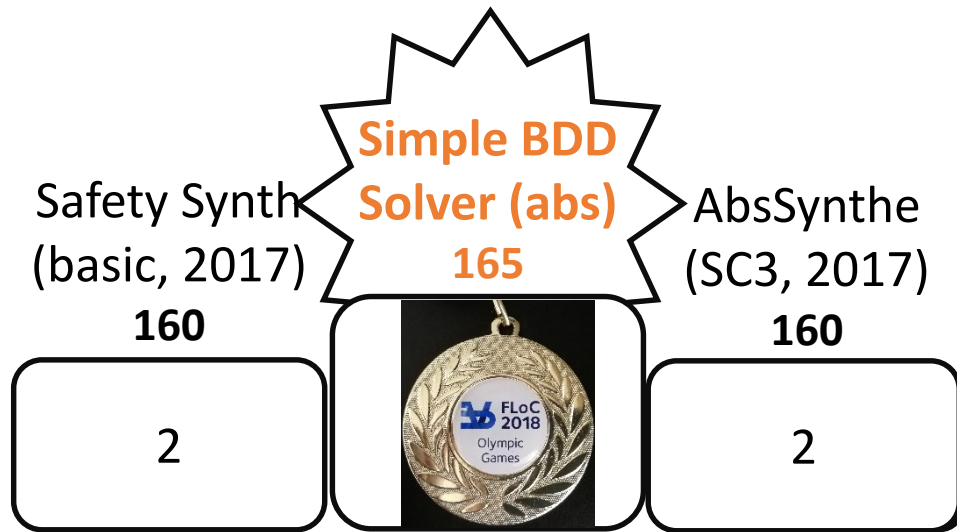
Hors concours:

- **SDD Solver** (Walker)
- **LazySynt** (Sakr)

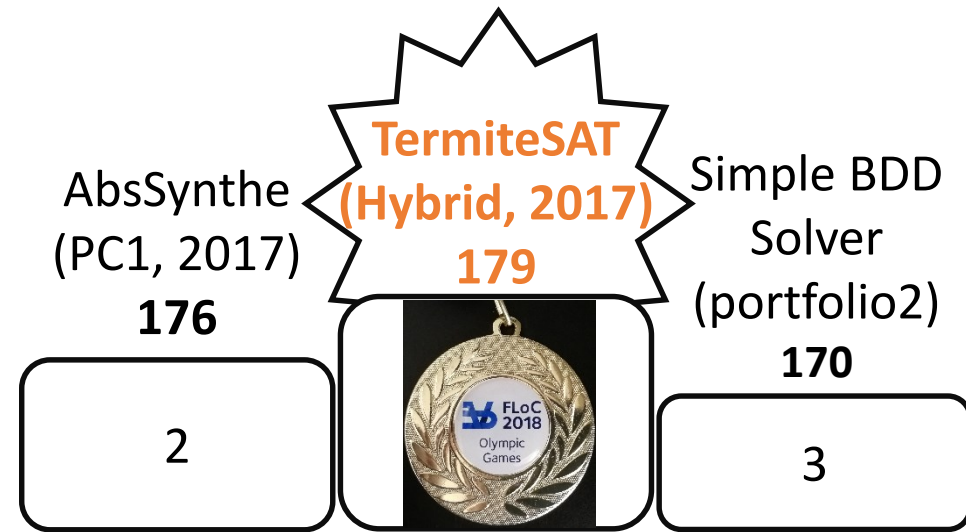


AI GER/Safety Results: Realizability (Number of Solved Instances)

Sequential mode (1 CPU hour, single core):



Parallel mode (1 hour wall time, 4 cores):

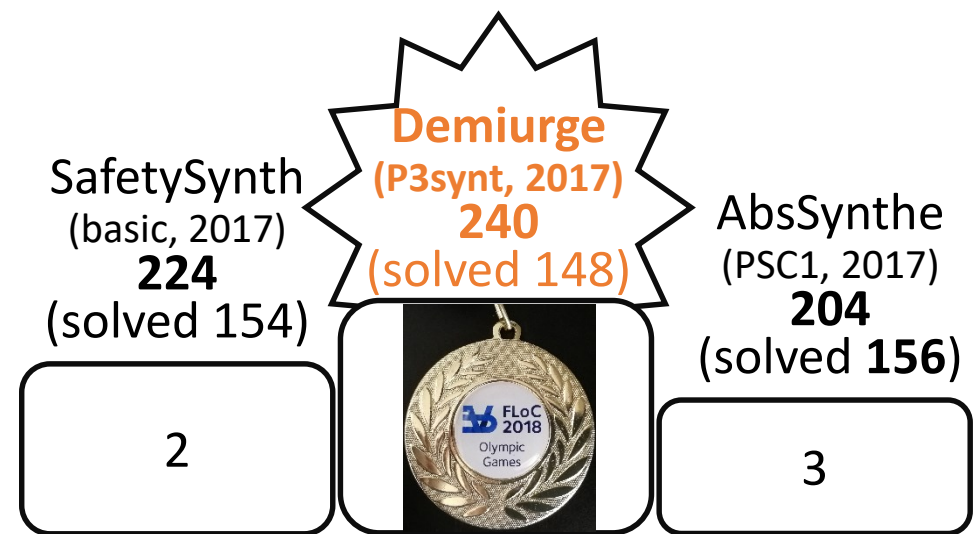


AI GER/Safety Results: Synthesis (Quality Ranking)

Sequential mode (1 CPU hour, single core):



Parallel mode (1 hour wall time, 4 cores):

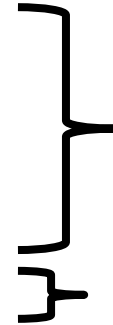


SYNTCOMP 2018: LTL (TLSF) TRACK

LTL (TLSF): Participants 2018

Updated:

- **BoSy** (Faymonville, Finkbeiner, Tentrup) [CAV17]
- **Bowser** (Klein) [CAV16]
- **Party/Kid** (Khalimov)
- **Itlsynt** (Colange, Michaud)



Based on different
notions/versions of
Bounded Synthesis
Presented before



New entrants:

- **Strix** (Meyer, Sickert, Luttenberger) [CAV18]:
 - decomposition of LTL formula (for efficient automata translation, using symmetry)
 - automata translation on demand (during game solving)
 - explicit-state game solving based on strategy iteration

LTL (TLSF): New Benchmarks 2018

Used in competition:

- Temporal Stream Logic (TSL) benchmarks (F. Klein, M. Santolucito)
- Some hardware components, parameterized (F. Klein)
- Infinite tic-tac-toe game (F. Klein)

Not in competition:

four problems from abstraction-based control synthesis, really big (Z. Liu, N. Ozay)

LTL (TLSF) Results: Realizability (Number of Solved Instances)

Sequential mode (1 CPU hour, single core):

Parallel mode (1 hour wall time, 4 cores):



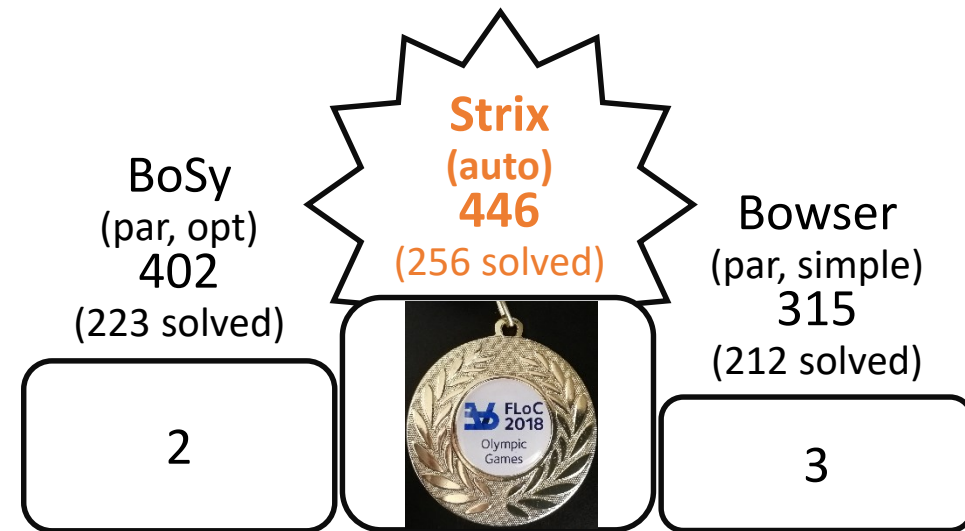
Total Instances: 286

LTL (TLSF) Results: Synthesis (Quality Ranking)

Sequential mode (1 CPU hour, single core):



Parallel mode (1 hour wall time, 4 cores):



3rd in quantity: Itlsynt (incr), 214 solved

LTL (TLSF) Results: Synthesis

	Solved	Unique	MC TO	Quality Points
BoSy (basic)	222	0	4	369
BoSy (opt)	205	0	5	368
Bowser (opt)	166	0	0	307
Bowser (simple)	206	0	0	306
Bowser (synth)	187	0	0	287
Itlsynt (ds)	211	0	23	247
Itlsynt (incr)	214	0	19	258
Itlsynt (sd)	210	0	23	246
Strix (basic)	247	0	17	384
Strix (labels)	257	6	6	410
Strix (min)	248	0	16	413
BoSy (par, basic)	223	0	12	371
BoSy (par, opt)	223	0	9	402
Bowser (par, opt)	162	0	0	302
Bowser (par, simple)	212	0	0	315
Bowser (par, synth)	194	0	0	300
Strix (par, auto)	256	0	6	446

Summary and Outlook

We are achieving our goals:

- significant improvement of tools in 5 years of SYNTCOMP
- thousands of benchmarks collected
- 13 different tools competed

Possible extensions/changes for next years:

- require counter-strategy if unrealizable?
- can we make life easier for LTL model checkers?
- add new tracks? need every track every year?
- define “challenge” benchmarks?

Winners of Safety Track:

	Sequential	Parallel
Realizability	Simple BDD Solver	TermiteSAT
Synthesis Quality	SafetySynth	Demiurge
Synthesis Quantity	SafetySynth	AbsSynthe

Winners of LTL Track:

	Sequential	Parallel
Realizability	Strix	Strix
Synthesis Quality	Strix	Strix
Synthesis Quantity	Strix	Strix

More details soon on
<http://www.syntcomp.org> and in the
competition report!